<u>**DRAWING AMENDMENTS:**</u>

Applicants respectfully submit a replacement drawing of Fig. 4A. The clock waves were mislabeled as 410 and should be 404. The replacement drawing fixes the mislabeled clock waves. No new matter is added with the drawing amendments.

REMARKS

With this Response, independent claims 9, 12, 13, 14, 17, 18, and 25 are amended. No claims are added or canceled. Therefore, claims 9-18 and 25-27 are pending.

CLAIM OBJECTIONS

Claims 25 and 27 are objected to because of informalities. Applicants amend claim 25. Claim 27 depends upon claim 25 and so by nature of dependency it inherits the amendment made in claim 25. Claim 26 was cancelled in the response filed on February 26, 2008. Therefore, Applicants respectfully request withdrawal of the claim objections.

REJECTIONS UNDER 35 U.S.C. § 101

Claims 9-18 are rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Particularly, the Examiner states that the "process" of instant claim 9 does not require any transformation and reduction of an article "to a different state or thing." *Office Action, Page 3*. Furthermore, the Examiner states that the "process" is not tied to a particular machine that transforms data in such a way to produce a useful, concrete, and tangible result. *Id.*

Applicants amend independent process claims 9 and 14 to clarify the patentable subject matter. As the claims are interpreted, it is important to realize that "[t]he claimed invention as a whole must be useful and accomplish a practical application" for it to satisfy the utility requirement of § 101. *MPEP 2106 page 2100-6 citing State Street Bank & Trust Co. v. Signature Financial Group Inc., 149 F.3d 1667, 1373-74 (Fed. Cir. 1998).* The following reasons highlight why claims 9 and 14 in their amended form satisfy the requirements of § 101.

I.   APPLICANTS' INVENTION HAS A CLEAR USEFUL PURPOSE THAT SATISFIES THE UTILITY REQUIREMENT OF § 101

Claims 9 and 14 are directed to measuring critical timing properties of an input/output circuit in an integrated circuits (IC) device that is used for determining whether a failure condition exists for the input/output circuit based on the measured timing properties i.e. setup and hold timing properties. The measurement technique involves inverting the clock after the strobe edge is pulled in by at least a clock phase, and then pushing the data out in predetermined steps while holding the strobe edge

constant. As an end product, claims 9 and 14 as amended produce a useful result in the form of a measured setup and hold timing parameter and a determination of a failure of the input/output circuit in an IC device.

II.   THE CLAIMED PROCESS CANNOT BE ACCOMPLISHED BY PAPERWORK BECAUSE IT
        REQUIRES NOVEL CIRCUITRY TO MEASURE TIMING PARAMETERS OF THE
        INPUT/OUTPUT CIRCUIT OF AN IC DEVICE THAT TRANSFORMS THE CLOCK
        SIGNAL, AND TO DETERMINE A FAILURE CONDITION IN THE CIRCUIT

        Examiner concludes that the subject matter of claims 9 and 14 "requires at most human thought and paperwork" and thus the claimed subject matter is not patentable under § 101. *Office Action, Page 3*.

        Neither claim 9 nor claim 14 fall within the judicial exceptions of § 101 i.e. laws of nature, natural phenomena, and abstract idea. Claims 9 and 14 recite the process of measuring critical timing properties of input/output circuits of an IC device that determines failure conditions of such circuits. In particular the process claims measure the setup and hold timing properties of input/output circuits. The measurement involves a series of *steps that transform* the clock signal by inverting the clock signal using novel circuitry. *See Fig 6. for transformation of IOPLLClk; See also Fig. 5 and Fig. 8 of application for circuits used in transforming the IOPLLClk (emphasis added)*. Therefore, the claimed "process is . . . an act, or a series of acts, performed upon the" clock signal which is the "subject matter to be transformed and reduced to a different state or thing." *Office Action, Page 3 citing Cochrane v. Deener, 94 U.S. 780, 788 (1877).*

        The setup and hold timing parameters measured by the claimed process that determines failure conditions in the circuit are not laws of nature because, unlike gravity, the timing parameters change in value depending upon operating conditions of the input/output circuit. The timing parameters are not natural phenomena either because the measured value by the claimed process depends upon design parameters of the man made circuit. Likewise, the timing parameters being measured by process claims 9 and 14 are not abstract ideas because for the parameters to be measured, novel circuit techniques described in the claims have to be utilized e.g. inverting the clock after pulling in the strobe edge, and holding the strobe edge constant while pushing the data out in

predetermined increments. Similarly, detecting failure of the input/output circuit based on the measured timing result is not an abstract idea or natural phenomena.

The claimed measuring technique that detects failure of the input/output circuits, thus, cannot be done using paperwork alone. Conversely, the claimed process, in one embodiment, requires a sophisticated delay line with multiplexed outputs, phase detector, control logic for phase alignment etc. *See Application, Fig. 5 and Fig 8*.

III.   THE CLAIMED PROCESS IS TIED TO AN INPUT/OUTPUT CIRCUIT WHICH IS A
         "MACHINE" UNDER § 101 THAT PRODUCES A USEFUL RESULT

Examiner concludes that the process claims 9 and 14 are not "tied to a particular *machine* that transforms data . . . to produce a useful, concrete, and tangible result," and so the claimed process is not a patentable subject matter under § 101. *Office Action, Page 3 (emphasis added)*.

The U.S. Supreme Court defined machines as "a concrete thing, consisting of parts, or of certain devices and *combination of devices*." *Burr v. Duryee, 68 U.S. 531, 570 (1863) (emphasis added)*. Both claims 9 and 14 are tied to at least one input/output circuit of an IC device. The steps of measuring the setup and hold timing parameters and detecting failures in the input/output circuit require pulling the strobe edge by predetermined decrements, inverting the clock, pushing the data etc. These steps transform the clock signal into several delayed clocks. The above steps are performed, in one embodiment, by circuits such as the delay line, phase detector, multiplexers, inverters, buffers etc. *See Application, Fig 5 and Fig 8*. These circuits consist of combination of devices and other circuits, and thus these circuits are a "machine" according to *Burr*.

Since the measuring process in claims 9 and 14 are tied to the circuit machine, the invention is within the patentable subject matter category of § 101. Additionally, claims 9 and 14 do recite "electrical" acts because the acts of inverting the clock, pulling the strobe edge, pushing the data etc. are acts that require, in one embodiment, electrical circuits like inverters, buffers, multiplexers, phase-detector, logic gates, controlled delay line etc. *Id*. Furthermore, the measured setup and hold parameter are products of the

circuit machine that characterize the input/output circuits by determining failure conditions in those circuits—a tangible result.

Based on the above arguments, Applicants traverse the rejections. The independent process claims 9 and 14 are well within the patentable subject matter. The process claims 9 and 14 are tied to electrical circuits that are a combination of devices (machines) that produce a useful result—setup and hold timing parameter of input/output circuits of an IC device, and a determination of failure condition of such circuits. Claims 10-13 and 15-18 depend from claims 9 and 14 respectively. By nature of dependency, claims 10-13 and 15-18 also satisfy the patentable subject matter requirement.

REJECTIONS UNDER 35 U.S.C. § 112

Examiner also rejects claims 9-18 under 35 U.S.C. § 112 ¶2, as being incomplete for omitting essential steps.

Applicants clarify the preamble of the independent method claims 9 and 14 by replacing "A method of testing" with "A method for measuring timing properties of at least one input/output circuit." The body of the claims following the preamble also recite the steps of measuring the setup and hold parameters of the input/output circuit of the IC device. The preamble and the body are now consistent with one another. Claims 10-13 and 15-18 depend from claims 9 and 14, and so by nature of dependency they also satisfy § 112 ¶2 requirement.

CONCLUSION

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, all pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Date: _____9/2/08_____

/Paul A. Mendonsa/ _____
Paul A. Mendonsa
Reg. No. 42,879
Attorney for Applicant

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

(503) 439-8778

5   BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to testing of I/O pins by utilizing an Alternating Current

(AC) I/O loop back testing in a source synchronous mode.

10

Description of the Related Art

As the technology for manufacturing integrated circuits advances, more logic

functions are included in a single integrated circuit device or a system on a chip (SoC).

15   Modern integrated circuit (IC) devices include large numbers of gates on a single

semiconductor chip, with these gates interconnected so as to perform multiple and

complex functions. The fabrication of an IC incorporating such Very Large Scale

Integration (VLSI) must be error free, as any manufacturing defect may prevent the IC

from performing all of the functions that an IC or SoC is designed to perform. Such

20   demands require verification of the design of the IC or SoC and also various types of

electrical testing after the IC or SoC is manufactured.

However, as the complexity of the ICs and SoCs increase, so does the cost and

complexity of verifying and electrically testing the individual IC or multiple ICs in a

system for a SoC. Testing , manufacturing costs and design complexity increase

25   dramatically because of the increasing number of functional pins on the integrated

devices and SoC. With the increased number of I/O pins on each integrated device or

system, the complexity and cost of testing each I/O pin has increased.

Verifying the functionality of an IC is typically accomplished by placing the IC

on a tester that includes a tester channel for each I/O pin on the IC. Subsequently, each

5   I/O buffer coupled to an I/O pin is tested for functionality, timing, performance, etc.

However, there are often problems associated with testing an IC in this manner. One

problem is that testing each I/O pin on an IC is time consuming and often expensive due

to test equipment costs. Another problem is that the speed of the test equipment is

typically not fast enough to keep pace with the IC. Moreover, existing test equipment is

10   not capable of testing high-speed source synchronous systems.

In order to solve the problems of exclusively using a tester to test an IC, several

contemporary testing schemes use the IC to assist in the testing. This process is

commonly referred to as an I/O loopback test. I/O loopback tests are typically carried out

15   by providing data from a functional logic block (or FLB) within the IC (e.g., a

microprocessor), and driving the data out through the output component of each I/O

buffer. Subsequently, the data is driven back through the input component of the I/O

buffer to the FLB in order to verify if correct data has been received or not.

Consequently, the IC verifies whether the input and output components of each I/O buffer

20   is functioning properly.

The problem with conventional I/O loopback tests, however, is data is driven on a

rising edge of a clock and strobe on a falling edge of the clock. Thus, the setup and hold

margins are calculated based on the trailing edge of the data. As depicted in ~~Figures~~ Figs

25   1 and 2, the loopback circuitry allows a strobe clock to be shifted (delayed) by one data

clock cycle. Typically, the strobe and data pads can not use the same clock and are

designed with excessive skew budget. Likewise, the delay lines consist of a large number

5   of devices while each strobe clock utilizes their own delay line. Furthermore, in die

variation from one delay line to another may cause measurement errors.   Thus, present

A/C I/O loopback testing that utilizes distributed delay pads results in inconsistencies due

to large skew budgets, measurement errors and increased manufacturing cost since the

strobe and data pads utilize different clock paths.

10

5

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

Subject matter is particularly pointed out and distinctly claimed in the concluding portion

of the specification. The claimed subject matter, however, both as to organization and

method of operation, together with objects, features, and advantages thereof, may best be

10   understood by reference to the following detailed description when read with the

accompanying drawings in which:

Figs. 1 and 2 illustrate the prior art.

Fig. 3 illustrates a method for a timing diagram as utilized by an embodiment.

Figs. 4A and 4B illustrate a method for a timing diagram as utilized by an

15   embodiment.

Fig. 5 illustrates a circuit for a varying duty cycle clock generation as utilized by

the embodiment depicted in either ~~Figure~~ Fig. 3 or Figs. 4A and 4B or both.

~~Figure~~ Fig. 6 is a timing diagram as utilized by an embodiment that was described

in connection with ~~Figure~~ Fig. 5.

20   Fig. 7 illustrates a circuit utilized in an embodiment .

~~Figure~~ Fig. 8 illustrates a circuit utilized in the embodiment described in

connection with ~~Figure~~ Fig. 7.

25

5   DETAILED DESCRIPTION OF THE INVENTION

A method and system for efficient clock generation within an integrated device or SoC are described. In the following description, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention.

An area of current technological development relates to reducing test complexity and cost. As previously described, DFT methods facilitate the testing of ICs and SoCs. However, A/C I/O loopback testing is not as efficient and accurate as needed because of the increased cost of separate clock paths for data and strobes and in die variation due to separate delay lines. In contrast, the claimed subject matter facilitates a method and apparatus that incorporates utilizing the same clock for data and strobe and utilizing a single delay line will decrease manufacturing cost, eliminates in die variation with respect to delay lines and reduces skew between data and clock. Also, the claimed subject matter facilitates measuring the setup and hold times based on a leading edge of the data and eliminates the need for delaying the strobe clocks. Thus, the claimed subject matter eliminates the need for delay cells in the strobe pads and decreases I/O clock skew, and results in higher data transfer rates. Furthermore, the improved accuracy reduces guard band for I/O and allows for supporting higher I/O frequencies In contrast, the prior art depicted in ~~Figures~~ Figs. 1 and 2 measured the setup and hold times based on a trailing edge of the data.

The claimed subject matter facilitates detecting failures by pulling (moving in) the strobe edge in predetermined decrements by changing the duty cycle of the clock. In

5   contrast, the prior art would push (delay) the strobe clock by utilizing delay cells. In one

embodiment, the circuitry and methods depicted in the following ~~figures~~ Figs. are

incorporated within a processor that may be utilized in a variety of applications, such as,

a personal digital assistant (PDA), cell phone, internet tablet, or computer.

Fig. 3 illustrates a method for a timing diagram as utilized by an embodiment. In

10   one aspect, the method facilitates utilizing a clock for both the data and strobe to measure

a setup and hold time for a plurality of input/output pads or pins for a test mode of

operation. In the same embodiment, the test mode of operation is an AC I/O Loopback

test mode of operation.

As described earlier, this test mode of operation utilizes detection of failures based on

15   adjusting the strobe clock. As previously described, the AC I/O loopback test is typically

carried out by providing data from a functional logic block (or FLB) within the IC (e.g., a

microprocessor), and driving the data out through the output component of each I/O

buffer. Subsequently, the data is driven back through the input component of the I/O

buffer to the FLB in order to verify to that the correct data has been received.

20   Consequently, the IC verifies whether the input and output components of each I/O buffer

is functioning properly.

Labels 302 and 304 depict a similar clock for both the data and strobe. In

contrast, the prior art utilized separate clocks for the data and strobe. Also, the setup and

hold times are calculated based on pulling in (moving in) the strobe clock (304) in

25   predetermined decrements up to a single phase for one embodiment. For example, the

decrements may be 120 picoseconds. However, the claimed subject matter is not limited

to 120 picosecond decrements. The claimed subject matter supports various decrement

5   value because the decrement value may differ based on the application and clock speed.

Therefore, the strobe falling edge is adjusted by changing the duty cycle of the clock,

instead of delaying the clock. Consequently, the failures are depicted by label ~~306~~ 310 to

indicate the characteristic setup and hold times of a plurality of input/output pins.

Therefore, the claimed subject matter utilizes the same clock for both data and strobe and

10 allows for central control and eliminates the need for delay cells in the destination pads.

Therefore, the claimed subject matter results in decreased die size and decreased power

consumption because of eliminating the need for delay cells. In contrast, the prior art

utilized distributed control that required delay cells in all destination pads.

As previously described for one embodiment, the strobe falling edge is moved in

15 up to a single phase. However, this embodiment may also allow for inverting the clock

after moving in the strobe edge for an entire single phase and the duty cycle is changed in

predetermined values toward 50%, which is discussed in connection with ~~Figures~~ Fig. 4A

and 4B. Alternatively, in another embodiment, the strobe falling edge is moved in up to a

value of a single phase with no other clock or duty ~~change~~ cycle changes.

20 Figs. 4A and 4B illustrate a method for a timing diagram as utilized by an

embodiment. As previously described, the figures depict an embodiment that may be

utilized with the embodiment described in connection with ~~Figure~~ Fig. 3 to allow for

inverting the clock after moving in the strobe edge for an entire single phase and the duty

cycle is changed in predetermined values toward 50%. For example, the inverted clock

25 holds the strobe edge constant and pushes (delays) the data edge.

~~Figure~~ Fig. 4A depicts the ability to pull the strobe in despite the pulling in of the

strobe edge up to a value of a single phase of the clock. Label 402 depicts the strobe

5   position after pulling it in for a single phase of the clock. Labels 406 and 408 depict the

data driving edge and strobe driving edge, respectively. Furthermore, label[[s]] 404

~~depict~~ depicts the clock wave when the strobe edge has already been pulled in for a value

of a single phase of the clock. The fail window 410 depicts the range of failures. Thus,

in one embodiment, the entire fail window can not be detected even when the strobe has

10   been pulled in for an entire single phase of the clock.

~~Figure~~ Fig. 4B depicts the clock being inverted and pushing out (delaying) the

data to detect the entire fail window while holding the strobe is at a fixed position. In one

embodiment, the strobe is at a fixed position that is pulled in a value of a single phase

clock. The data is pushed out by pushing out the rising edge of the clock, as depicted by

15   clock labels 412, 414, 416, and 418. Also, the strobe driving edge 420 remains constant

while the data driving edge 422 changes for each clock label 412, 414, 416, and 418.

Thus, in one embodiment, the entire fail window is detected.

Fig. 5 illustrates a circuit for a varying duty cycle clock generation as utilized by

the embodiment depicted in either ~~Figure~~ Fig. 3 or Figs. 4A and 4B or both. For

20   example, the circuit allows for pulling in the strobe (as depicted in connection with

~~Figures~~ Fig. 3 and 4A) and delaying (pushing out) the data rising edge as depicted in

~~Figure~~ Fig. 4B.

The circuit receives an input of a clock for a plurality of Input/Output pins or

pads. In one embodiment, the clock has a duty cycle of 50% and is referenced by a name

25   of ~~IOPPLLClk~~ IOPLLClk. In a normal mode of operation of the integrated device or

system, the ~~IOPPLLClk~~ IOPLLClk is passed through an AND gate 502. Meanwhile, a

multiplexer 504 selects VCC during a normal mode of operation and a resulting output

of the AND gate 502 is ~~Data-Clk~~ Data-clk. Consequently, the ~~Data-Clk~~ Data-clk is

substantially similar to the ~~IOPPLLClk~~ IOPLLClk during normal mode of operation.

      In contrast, during a test mode of operation, such as, I/O Loopback mode, the duty

cycle of the ~~Data-Clk~~ Data-clk is varied based at least in part on the Multiplexer 504.

For example, a plurality of delay elements 506 (B,C,D,E,Fand G) are controlled by a

control unit 508. Furthermore, the control unit receives an input from the phase detector

~~510~~ 520 based at least in part on the ~~IOPLLCLK~~ IOPLLClk and the delayed clock thru

the final delay element G. As IOPLLClk is inverted by an inverter A, the plurality of

delayed versions (outputs of B,C,D,E,F and G) of the inverted ~~IOPLLCLK~~ IOPLLClk is

tapped and forwarded to the Multiplexer 504. The plurality of delayed versions are

further illustrated in connection with ~~Figure~~ Fig. 6. In one embodiment, the multiplexer

responds to a predetermined bit pattern from a scan chain. Also, the phase detector and

control logic supervise and insure that the output from the delay chain is one phase of the

~~IOPPLLCLK~~ IOPLLClk by modulating the delay of each of the plurality of delay

elements. Thus, based on the multiplexer select, one of the plurality of delayed versions

of the inverted ~~IOPLLCLK~~ IOPLLClk is forwarded to the AND Gate 502.

Consequently, the ~~Data-CLK~~ Data-clk is then inverted and forwarded to another

multiplexer 512. The multiplexer 512 select is based on a signal, stb_pull, which is a

logic high during the pulling in of the strobe, "strobe pull"~~[[)]]~~. Consequently, the

multiplexer 512 forwards the ~~Data-Clk~~ Data-clk while the strobe pull is active.

Otherwise, the multiplexer 512 forwards the inverted version of ~~Data-Clk)~~ Data-clk.

Subsequently, the ~~Data-Clk~~ Data-clk is forwarded to the input/output pads and is used to

generate the data/strobe clock.

5   ~~Figure~~ Fig. 6 is a timing diagram as utilized by an embodiment that was described

in connection with ~~Figure~~ Fig. 5. The timing diagram depicts the delay line and

generation of a non-50% duty cycle data clock as described in connection with the circuit

of ~~Figure~~ Fig. 5. Label A depicts the inverted ~~IOPLLCLK~~ IOPLLClk. Label B depicts

the output of delay element B of ~~Figure~~ Fig. 5; Label C depicts the output of delay

10   element C of ~~Figure~~ Fig. 5; Label D depicts the output of delay element D of ~~Figure~~ Fig.

5; Label E depicts the output of delay element E of ~~Figure~~ Fig. 5; Label F depicts the

output of delay element F of ~~Figure~~ Fig. 5; and Label G depicts the output of delay

element G of ~~Figure~~ Fig. 5.

        ~~Figure~~ Fig. 7 is a circuit of an embodiment. The circuit may be utilized with the

15   previous embodiments depicted in the previous ~~Figures~~ figures to improve measurement

accuracy. For example, measurement accuracy could be compromised because the data

and strobe edge did not line up when the strobe edge was pulled in by a clock cycle.

Thus, there could be a measurement inaccuracy of a single delay cell. ~~Figure~~ Fig. 7

improves the measurement accuracy by a plurality of multiplexers ~~702~~ 712, 704, and 706.

20   An output of multiplexer 706 is for generating a strobe clock, while the other two

multiplexers are for generating a data clock.   The multiplexers receive the clock,

~~DATA CLK~~ Data-clk generated by ~~Figure~~ Fig. 5, at one input of a logic 0 select port.

The multiplexers 704 and ~~702~~ 712 only receive one input. In contrast, multiplexer 706

receives a single delayed version of the ~~DATA CLK~~ Data-clk from delay cell 708 and

25   the mux select is enabled by whether the data is being delayed (Push data, which was

described in connection with ~~Figure~~ Fig. 4B).

5   The operation of ~~Figure~~ Fig. 7 depends on whether the strobe pull is active or

whether the data push is active. For example, the multiplexer 706 forwards the non-

delayed version of the ~~dATa-clk~~ Data-clk (logic 0 port) during strobe pull because the

Push data multiplexer select has a value of logic 0. In contrast, the multiplexer 706

forwards the delayed version of the ~~dATa-clk~~ Data-clk (logic 1 port) during push data

10   (moving the rising edge of data) because the Push data multiplexer select has a value of

logic 1. Thus, ~~Figure~~ Fig. 7 facilitates the clock generation at the data and strobe drivers

to be synchronized (lined up) for the rising of the data clock and falling of the strobe

clock).

       ~~Figure~~ Fig. 8 depicts the entire circuit of the embodiment described in connection

15   with ~~Figure~~ Fig. 7 by combining the circuits of ~~Figure~~ Fig. 5 and 7. Alternatively, in

another embodiment, ~~Figure~~ Fig. 5 is only utilized without the circuitry of ~~Figure~~ Fig. 7.